Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAHUL RAZDAN, JAMES B. KELLER,
and RICHARD E. KESSLER

Appeal No. 2001-2477
Application No. 09/099,384

ON BRIEF

Before HAIRSTON, BARRETT, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2 and 4 through 24.

The disclosed invention relates to a method and apparatus for maintaining cache coherence in a multiprocessor system that has a plurality of cache and a main memory.

Claims 1 and 12 are the only independent claims on appeal, and they read as follows:

1. A multiprocessor computer system, comprising:

a cache comprising a plurality of blocks, each block having a coherence state;

an external unit generating a request to modify one of the blocks of the cache, the request being generated as a function of the coherence state of the block;

a memory management system managing said cache, wherein said memory management system does not internally duplicate the coherence state of the cache;

wherein said memory management system receives the request to modify one of the blocks and sends an acknowledgment to the external unit in response to the request to modify, the acknowledgment being determined to be one of grant permission and denial of permission based on a state of the cache; and

wherein the external unit modifies the block of the cache only if an acknowledgment granting permission is received responsive to the request.

12. A method of maintaining cache coherence in a multiprocessor system having a plurality of caches and a main memory, comprising the steps of:

sending a request to modify a block of a first cache of the plurality of caches, the request corresponding to a coherence state of the block of the first cache;

determining if said block exists in a dirty form in any other of the plurality of caches by directly probing those caches;

receiving an acknowledgment responsive to the request indicating one of a grant and denial of permission to modify the block of the first cache based on said determination step; and

modifying the block of the first cache if the acknowledgment grants permission.

No references were relied on by the examiner in the rejection on appeal.

Claims 1, 2, and 4 through 24 stand rejected under the first paragraph of 35 U.S.C. § 112 for lack of written description of the phrase "wherein said memory management system does not internally duplicate the coherence state of the cache" (claim 1), and the phrase "determining if said block exists in a dirty form in any other of the plurality of caches by directly probing those caches" (claim 12).

Reference is made to the briefs (paper numbers 12 and 14) and the answer (paper number 13) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the lack of written description rejection of claims 1, 2 and 4 through 11, and we will reverse the lack of written description rejection of claims 12 through 24.

Appellants argue (brief, pages 6 through 9; reply brief, pages 1 through 4) that the prior art (U.S. Patent No. 5,634,068 to Nishtala) discloses a memory management system (i.e., a system controller 100) that uses "duplicate cache tags," and that one of ordinary skill in the art would recognize that their specification describes a system where the memory management system need not maintain duplicate cache tags.

For an answer to both of appellants' arguments, we turn to In re Wohnsiedler, 315 F.2d 934, 937, 137 USPQ 336, 339 (CCPA 1963) which states:

> Though prior art may be used to show what matters would lie within the knowledge of one skilled in the art to explain ambiguities in an application, it cannot be used to supply specific limitations not found therein. The question is not what modification of appellants' disclosure might occur to one skilled in the art, it is rather whether the invention they are claiming is *described* in their specification.

Appellants pose the question (reply brief, page 3) "[a]re the Applicants' required to mention duplicate cache tags if one of ordinary skill in the art is already well aware of those concepts?" If that is their invention, then the answer is yes. Notwithstanding the awareness of the skilled artisan, appellants must describe in the disclosure their contribution to the art pertaining to "duplicate cache tags" or the lack of such cache tags in the memory management system. Thus, we agree with the examiner's position (answer, page 3) that "the specification does NOT disclose that the memory management system does *not* internally duplicate the coherence state of the cache," and the rejection of claims 1, 2 and 4 through 11 is sustained because "the negative limitations recited in the present claims, which did not appear in the specification as filed, introduce new concepts and violate the description requirement of the first paragraph of 35 U.S.C. 112." Ex parte Grasselli, 231 USPQ 393, 394 (Bd. App. 1983), aff'd mem., 738 F.2d 453 (Fed. Cir. 1984).

Turning to claim 12, the examiner is of the opinion (answer, pages 6 and 7) that the claim lacks written description support for "directly probing" the caches because the microprocessor is probed directly, and then the microprocessor in turn "indirectly" determines the contents of the caches. Claim 12 on appeal is drafted in a method format, as opposed to a system format, and does not specify what portion of the system is responsible for "directly probing" the caches. In other words, nothing in claim 12 precludes the memory management unit from directly probing the

microprocessor which, in turn, directly probes the caches. The lack of written description support rejection of claims 12 through 24 is, therefore, reversed because appellants' disclosure (specification, pages 26, 29, 34, 41, 42) clearly provides written description support for the questioned phrase by stating that the microprocessor 20 executes the probe command by locating the block in its cache.

DECISION

The decision of the examiner rejecting claims 1, 2 and 4 through 24 under the first paragraph of 35 U.S.C. § 112 is affirmed as to claims 1, 2 and 4 through 11, and is reversed as to claims 12 through 24. Accordingly, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

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